REMARKS

The Examiner is thanked for the thorough examination of the present application, and suggestions set forth in the Office Action. The Office Action, however, tentatively rejected all claims 1-40. Applicant respectfully requests reconsideration in view of the amendments and remarks set forth herein. Among these amendments, the features of claim 3 have been incorporated into claim 1 (and claim 3 has been correspondingly canceled).

Response To Drawing Objections

The drawings were objected to for certain inconsistencies between the specification and the drawings. Replacement sheets are included in this response to correct the inconsistency between the specification and the drawings. Especially, labels T_1 and T_2 in Fig. 2 are interchanged as the Examiner has recommended, and "$5.6x10^9$" of Example III in Attachment is changed into "$5.6x10^8$."

The Applicant believes that the drawings reflected in the replacement sheets overcome the objection.

Response To Claim Objections

Claims 12, 27, and 39 were objected in the Office Action because of certain informalities. Claims 12, 27, and 39 are amended herein to be consistent with the specification, and Applicant believes that the amendment adds no new matter to the application.

Response To Claim Rejections Under 35 U.S.C. §102

Claims 1-4, 6, 7, 11, 13-18, 20, 21, 26, 28-31, 33, 34, 38 and 40 stand rejected under 35 U.S.C. §102(b) as allegedly anticipated by Bao at al (U.S. Patent No. 6455417). Applicant respectfully traverses this rejection on the grounds that the cited reference does not teach all limitations in the original claim 3, which has been incorporated into amended claim 1.

As amended, claim 1 cites:

> 1. A semiconductor device, comprising:
> a semiconductor substrate;
> a first metal layer formed overlying the semiconductor substrate;
> an etch stop layer formed overlying the first metal layer and the semiconductor substrate;
> a dielectric layer formed overlying the etch stop layer; and
> a second metal layer penetrating the dielectric layer and the etch stop layer and electrically connected to the first metal layer;
> wherein, **the etch stop layer has a dielectric constant smaller than 3.5**;
> wherein, **the dielectric layer has a dielectric constant smaller than 3.0**; and
> wherein **the dielectric layer has a tensile stress approximating to the compressive stress of the etch stop layer.**

(*Emphasis added*).

The Office Action (see page 4) rejected the original claim 3 (now claim 1) by alleging certain inherent properties of SiCN and spin-on-glass.

The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993) (reversed rejection because inherency was based on what would result due to optimization of conditions, not what was necessarily present in the prior art); *In re Oelrich*, 666 F.2d 578, 581-82, 212 USPQ 323, 326 (CCPA 1981). "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by

persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.' " *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999)

The Bao reference does not disclose anything about stress. As is understood by persons skilled in the art, the stress of a spin-on-glass layer depends on its forming recipe. The same thing is also true for a SiCN film. The Attachment (Table 1) in this application also provides several examples in which an etch stop layer has a compress stress not approximating the tensile stress of a dielectric layer. For the Examiner's reference, Applicant has provided for attachments hereto (Attachment A, Attachment B, Attachment C, and Attachment D), which are papers discussing the properties of some SOG and SiCN films used in semiconductor industry. Table 1 of "Characterization and Integration of Porous Extra Low-K Dielectrics" (Attachment A) discloses a SOG film with a stress of 21 MPa. Table 1 of "Cu/LKD-5109 Damascene Integration Demonstration Using FF-02 Low-k Spin-on Hard-mask and Embedded Etch-stop" (Attachment B) teaches two SOG films with stresses of 21 and 65 MPa. Table 1 of "Film Characterization of Cu Diffusion Barrier Dielectrics for 90 nm and 65 nm Technology Node Cu Interconnects" (Attachment C) teaches a SiCN film with stress of –200 Mpa. Finally, Table 1 of "Alleviating Electromigration Through Re-Engineering The Interface Between Cu & Dielectric-Diffusion-Barrier In 90 nm Cu/SiOC (k=2.9) Device" (Attachment D) discloses SiCN films with stresses ranged from -1.47E+9 to –1.69E+9. Taking consideration of the teachings of all these documents, it is clear the SiCN film in the Bao reference may have or may not have a compressive stress approximating to the tensile stress of the spin-on-glass film in the Bao reference. Stated another way, the stress match claimed in the amended claim 1 is not

necessarily present within Bao. Thus, it cannot be said to be "inherent" in Bao, as alleged by the Office Action. Accordingly, and for at least this reason the rejection should be withdrawn.

Neither the Lu reference (US PG Pub 2002/0100693) nor the Li reference (US patent 6753260), cited in the Office Action discuss the stress match, as claimed in amended claim 1. Thus, these references do not teach the claimed subject matter either.

While reducing the dielectric constants of the etch stop layer and the dielectric layer, this application diminishes the stress difference therebetween and achieves good reliability of the copper dual damascene structure (as mentioned in page 9, Ln 5-9 of this application). No prior art reference of record has recognized and diminished the stress difference between two low-k films as this application has achieved.

For at least the foregoing reasons, Applicant respectfully submits that claim 1 (as amended) is allowable over the cited references of record and respectfully requests that the rejection be withdrawn.

Independent claim 14, as amended, recites:

> 14. A copper damascene structure, comprising:
> a semiconductor substrate;
> a first copper layer formed overlying the semiconductor substrate;
> an etch stop layer formed overlying the first copper layer and the semiconductor substrate;
> a dielectric layer formed overlying the etch stop layer, in which a damascene opening is formed to penetrate the dielectric layer and the etch stop layer to expose the first copper layer; and
> a second copper layer formed in the damascene opening and electrically connected to the first copper layer;
> wherein, **the etch stop layer has a dielectric constant smaller than 3.5;**
> wherein, **the dielectric layer has a dielectric constant smaller than 3.0**; and
> wherein **the dielectric layer has a tensile stress approximating to the compressive stress of the etch stop layer.**

(*Emphasis added*).

Independent claim 29, as amended, recites:

> 29. A fabrication method for a semiconductor device, comprising the steps of:
>
> providing a semiconductor substrate having a first metal layer;
>
> forming an etch stop layer overlying the first metal layer and the semiconductor substrate, wherein **the etch stop layer has a dielectric constant smaller than 3.5**;
>
> forming a dielectric layer overlying the etch stop layer, wherein **the dielectric layer has a dielectric constant smaller than 3.0**;
>
> forming an opening which penetrates the dielectric layer and the etch stop layer and exposes the first metal layer; and
>
> forming a second metal layer in the opening, in which the second metal layer is electrically connected to the first metal layer;
>
> **wherein the dielectric layer has a tensile stress approximating to the compressive stress of the etch stop layer.**

(*Emphasis added*)

Both independent claims 14 and 29 have the similar distinguishing features as claim 1 and therefore define over the cited art for at least the same reasons.

Dependent Claims:

Dependent claims 2, 4-13, 15-16, 18-28, 30-41 are believed to be allowable for at least the reason that these claims depend from allowable independent claims 1, 14 and 29. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988).

New Claim

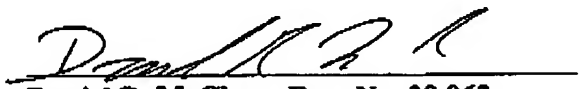
Claim 41 has been newly added to emphasize a recipe to manufacture an etch stop film having a low-K dielectric and a compressive stress approximating the tensile stress of a SOG film thereon. There is no cited prior art disclosing such a recipe and achieving such an

unexpected result. Therefore, beside its dependency from the independent claim 29, claim 41 should be allowable.

CONCLUSION

In light of the foregoing amendments and for at least the reasons set forth above, Applicant respectfully submits that all objections and/or rejections have been traversed, rendered moot, and/or accommodated, and that the now pending claims 1-2 and 4-41 are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned agent at (770) 933-9500.

Respectfully submitted,



Daniel R. McClure, Reg. No. 38,962

THOMAS, KAYDEN, HORSTEMEYER & RISLEY, L.L.P.
Suite 1750
100 Galleria Parkway N.W.
Atlanta, Georgia 30339
(770) 933-9500

Annotated Drawing Sheet

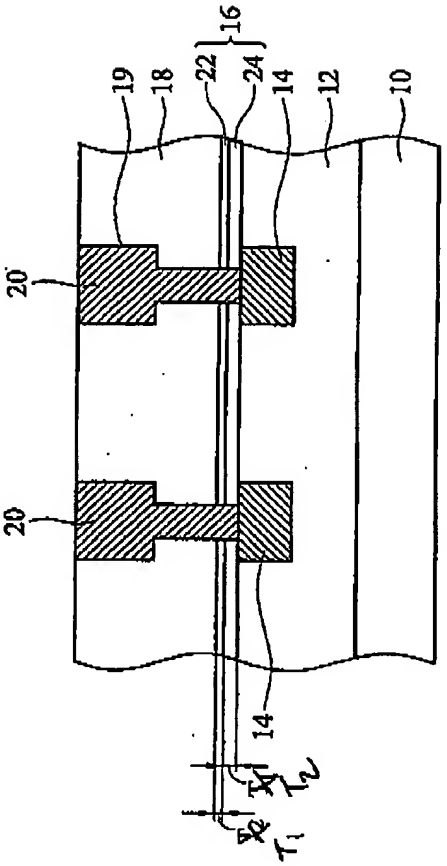


FIG. 2

Annotated Drawing Sheet

	Film Properties	Example I	Example II	Example III	Example IV
Low-k IMD layer	K_{IMD} value	3.0	2.5	2.5	2.2
	tensile Stress (dynes/cm^2)	5.0×10^8	4.0×10^8	4.0×10^8	1.7×10^8
	Hardness (Gpa)	2.2	0.84	0.84	0.13
	Modulus (Gpa)	15	8.4	8.4	3.7
ES layer	K_{ES} value	4.5	4.5	3.0	4.5
	compressive Stress (dynes/cm^2)	2.2×10^9	2.2×10^9	5.6×10^8	2.2×10^9
Relative RC delay		1.3	1.11	1.05	1.0

ATTACHMENT
Table 1